AVIONICS INTERFACE TECHNOLOGIES
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PCI-C664-V2

ARINC 664 Part 7 Test & Simulation Module for PCI

AIT's PCI-C664-V2 Test & Simulation module provides a PCI/PCI-X interface capable of supporting the simulation of multiple ARINC 664 End Systems within a single slot. The module supports both the conventional 10/100 Mbit/s ARINC 664 Part 7 Ethernet interfaces as well as the next generation 1 Gbit/s Ethernet interface.

The PC-C664-V2 utilizes two Small Form Factor Pluggable modules (SFPs) in order to provide the capabilities to support both traditional copper Ethernet interfaces as well as high speed optical physical connections. Using an FPGA based architecture, with multiple embedded processors, the PCI-C664-V2 module provides onboard support for upper layer protocol processing (ARINC 653, UDP, IP) and utilizes DMA to provide optimal data throughput. All ARINC 664 protocol operations, including VL traffic shaping, redundancy management, and IP fragmentation and reassembly, are handled onboard and require no host loading.

SOFTWARE SUPPORT

AIT's PCI-C664-V2 module is supported by AIT's ARINC 664 Software Development KIT (SDK) for Windows (XP, 7, 8, 10) and Linux (Ubuntu & CentOS). It provides a robust Application Programmer's Interface (API) for read/write access to the messaging ports and status information of the hardware module. Configuration of the simulated ARINC 664 End Systems (including the input/output VLs, upper protocol layers, and Sampling & Queuing message ports) is made easy with AIT's simple and intuitive XML based configuration data and Flight Simulyzer™ GUI application. The PCI-C664-V2 is also compatible with AIT ARINC 615A Software Data Loader tools allowing the module to be used for data loading target LRUs.

INPUT OPERATIONS

AIT's PCI-C664-V2 module provides full onboard support for ARINC 664 integrity checking and redundancy management operations. These operations can be individually configured for each input VL, providing a flexible approach that supports a wide variety of data acquisition and analysis applications. In addition to supporting up to 512 input VLs the module can also be configured to operate in promiscuous mode to capture all network traffic. All captured data is time tagged with a 8 nS resolution.

The IP, UDP, and ARINC 653 upper protocol layers are fully

Key Features

- Supports IEEE 802.3 10/100/1000 Mbit/s Full-Duplex Ethernet links
- Utilizes SFP's to support both copper and optical interfaces
- Simulates multiple ARINC 664 End Systems, including VL traffic shaping and input VL redundancy management
- Standard Ethernet operations simultaneous to ARINC 664 operations
- Supports up to 128 Output VLs and 512 Input VLs
- Supports up to 1024 Sampling & Queuing output message ports and up to 4096 input Sampling & Queuing message ports
- Upper layer protocol handling (ARINC 653, UDP, IP) managed onboard
- Provides DMA for high data rate applications
- Time-stamping of all received messages with 8 nS resolution
- Optional "promiscuous" mode allows capture of all network traffic for protocol analysis and data logging applications
- Windows XP/7/8/10, Linux, and LabVIEW Real Time Drivers & APIs provided (other OS support on request)
- Easy setup and configuration using AIT's Flight Simulyzer™ GUI and ARINC 664 End System configuration tools

managed onboard the PCI-C664-V2. IP reassembly is fully managed by the module and requires no host loading or memory resources. The module supports up to 4096 input message ports. Each message port can be configured as ARINC 653 Sampling & Queuing ports, UDP Service Access Ports (SAP), IP Ports, or MAC ports providing the test application a flexible approach, allowing error detection and access to all protocol layers. The incoming messages to each port are buffered onboard and require no host resources.

OUTPUT OPERATIONS

The PCI-C664-V2 module allows the simulation of multiple ARINC 664 End Systems. The module can be configured to handle ARINC 664 VL traffic shapping for up to 128 output VLs. For each VL the source (MAC) address is individually configurable allowing output traffic to emulate multiple source End Systems.

The IP, UDP, and ARINC 653 upper protocol layers are fully managed onboard the PCI-C664-V2. IP fragmentation is managed by the module, as well as VL sequence numbers and redundant data transmission, with no additional host loading.

The configuration and use of up to 1024 output message ports is supported. The message ports can be configured as ARINC 653 Sampling & Queuing ports, UDP Service Access Ports (SAP), IP Ports, or MAC ports providing access to all protocol layers in support error injection and flexible output operations.

Optionally, the module may be used in a replay mode to re-transmit previously captured network traffic. In addition to ARINC 664 output operations, the PCI-C664-V2 also supports the simultaneous output of standard Ethernet frames.

ORDERING INFORMATION

PCI-C664-V2

Half-size PCI modules (32-bit, 5V Tolerant) ARINC 664/Ethernet module for PCI 10/100/1000-BASE-T (uses copper RJ-45 connector) Ethernet Network A/B Interface

PCI-C664-V2-O

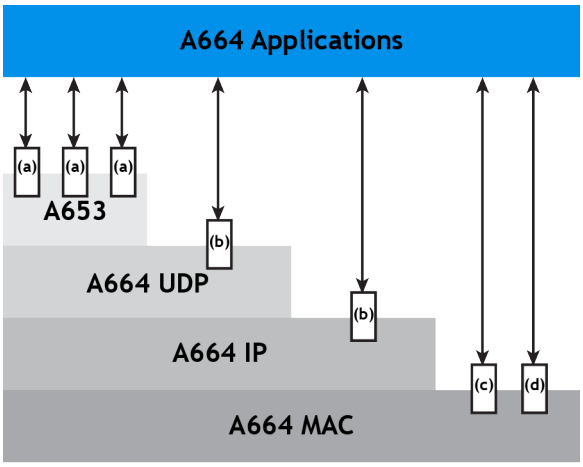
ARINC 664/Ethernet module for PCI 1000BASE-SX (uses 850nm optical LC connector) Ethernet Network A/B Interface

PCIx-C664-V2

Half-size PCI-X 3.3v, 64-bit module ARINC 664/Ethernet module for PCI-X 10/100/1000-BASE-T (uses copper RJ-45 connector) Ethernet Network A/B Interface

PCIx-C664-V2-O

ARINC 664/Ethernet module for PCI-X 1000BASE-SX (uses 850nm optical LC connector) Ethernet Network A/B Interface



(a) Sampling & Queuing Comm Ports (A653)
(b) UDP Service Access Point (SAP)
(c) MAC SAP
(d) COTS Ethernet

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PCIe-C664-V2

ARINC 664 Part 7 Test & Simulation Module for PCI

AIT's PCIe-C664-V2 Test & Simulation module provides a PCI Express (PCIe) interface capable of supporting the simulation of multiple ARINC 664 End Systems within a single slot. The module supports both the conventional 10/100 Mbit/s ARINC 664 Part 7 Ethernet interfaces as well as the next generation 1 Gbit/s Ethernet interface.

The PCIe-C664-V2 utilizes two Small Form Factor Pluggable modules (SFPs) in order to provide the capabilities to support both traditional copper Ethernet interfaces as well as high speed optical physical connections. Using an FPGA based architecture, with multiple embedded processors, the PCIe-C664-V2 module provides onboard support for upper layer protocol processing (ARINC 653, UDP, IP) and utilizes DMA to provide optimal data throughput. All ARINC 664 protocol operations, including VL traffic shaping, redundancy management, and IP fragmentation and reassembly, are handled onboard and require no host loading.

SOFTWARE SUPPORT

AIT's PCIe-C664-V2 module is supported by AIT's ARINC 664 Software Development KIT (SDK) for Windows (XP, 7, 8 & 10) and Linux (Ubuntu & CentOS). It provides a robust Application Programmer's Interface (API) for read/write access to the messaging ports and status information of the hardware module. Configuration of the simulated ARINC 664 End Systems (including the input/output VLs, upper protocol layers, and Sampling & Queuing message ports) is made easy with AIT's simple and intuitive XML based configuration data and Flight Simulyzer™ GUI application. The PCIe-C664-V2 is also compatible with AIT ARINC 615A Software Data Loader tools allowing the module to be used for data loading target LRUs.

INPUT OPERATIONS

AIT's PCIe-C664-V2 module provides full onboard support for ARINC 664 integrity checking and redundancy management operations. These operations can be individually configured for each input VL, providing a flexible approach that supports a wide variety of data acquisition and analysis applications. In addition to supporting up to 512 input VLs the module can also be configured to operate in promiscuous mode to capture all network traffic. All captured data is time tagged with a 8 nS resolution.

The IP, UDP, and ARINC 653 upper protocol layers are fully

Key Features

- Supports IEEE 802.3 10/100/1000 Mbit/s Full-Duplex Ethernet links
- Utilizes SFP's to support both copper and optical interfaces
- x4 PCI Express module
- Simulates multiple ARINC 664 End Systems, including VL traffic shaping and input VL redundancy management
- Standard Ethernet operations simultaneous to ARINC 664 operations
- Supports up to 128 Output VLs and 512 Input VLs
- Supports up to 1024 Sampling & Queuing output message ports and up to 4096 input Sampling & Queuing message ports
- Upper layer protocol handling (ARINC 653, UDP, IP) managed onboard
- Provides DMA for high data rate applications
- Time-stamping of all received messages with 8 nS resolution
- Time synchronizaiton to external devices using IRIG B
- Optional "promiscuous" mode allows capture of all network traffic for protocol analysis and data logging applications
- Windows XP/7/8/10, Linux, and LabVIEW Real Time Drivers & APIs provided (other OS support on request)
- Easy setup and configuration using AIT's Flight Simulyzer™ GUI and ARINC 664 End System configuration tools

managed onboard the PCIe-C664-V2. IP reassembly is fully managed by the module and requires no host loading or memory resources. The module supports up to 4096 input message ports. Each message port can be configured as ARINC 653 Sampling & Queuing ports, UDP Service Access Ports (SAP), IP Ports, or MAC ports providing the test application a flexible approach, allowing error detection and access to all protocol layers. The incoming messages to each port are buffered onboard and require no host resources.

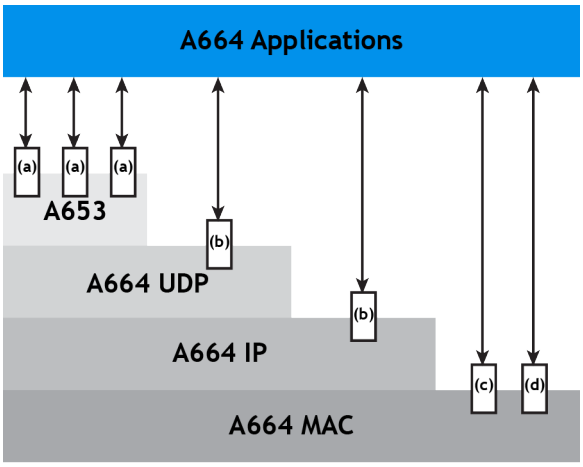
OUTPUT OPERATIONS

The PCIe-C664-V2 module allows the simulation of multiple ARINC 664 End Systems. The module can be configured to handle ARINC 664 VL traffic shapping for up to 128 output VLs. For each VL the source (MAC) address is individually configurable allowing output traffic to emulate multiple source End Systems.

The IP, UDP, and ARINC 653 upper protocol layers are fully managed onboard the PCIe-C664-V2. IP fragmentation is managed by the module, as well as VL sequence numbers and redundant data transmission, with no additional host loading.

The configuration and use of up to 1024 output message ports is supported. The message ports can be configured as ARINC 653 Sampling & Queuing ports, UDP Service Access Ports (SAP), IP Ports, or MAC ports providing access to all protocol layers in support error injection and flexible output operations. Optionally, the module may be used in a replay mode to re-transmit previously captured network traffic.

In addition to ARINC 664 output operations, the PCIe-C664-V2 also supports the simultaneous output of standard Ethernet frames.



(a) Sampling & Queuing Comm Ports (A653)
(b) UDP Service Access Point (SAP)
(c) MAC SAP
(d) COTS Ethernet

ORDERING INFORMATION

PCIe-C664-V2

ARINC 664/Ethernet module for PCI Express 10/100/1000-BASET (uses copper RJ-45 connector) Ethernet Network A/B Interface

PCIe-C664-V2-O

ARINC 664/Ethernet module for PCI Express 1000BASE-SX (uses 850nm optical LC connector) Ethernet Network A/B Interface

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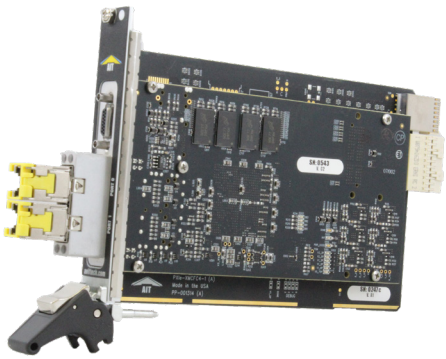
PXIe-C664-V2

ARINC 664 Part 7 Test & Simulation Module for Compact PXI Express

AIT's PXIe-664-V2 Test & Simulation module provides a PXI Express interface module capable of supporting the simulation of multiple ARINC 664 End Systems within a single slot and capable of recording and replaying ARINC 664/ Ethernet network data streams. The module supports both the conventional 10/100 Mbit/s ARINC 664 Part 7 Ethernet interfaces as well as the next generation 1 Gbit/s Ethernet interface. The module also provides support for IRIG-B time synchronization allowing the correlation of data timestamps accross multiple modules and system chassis.

The PXIe-664-V2 utilizes two Small Form Factor Pluggable modules (SFPs) in order to provide the capabilities to support both traditional copper Ethernet interfaces as well as high speed optical physical connections. Using an FPGA based architecture, with two dedicated embedded processors, the PXIe-C664-V2 module provides onboard support for upper layer protocol processing (ARINC 653 S&Q, UDP, IP) and utilizes DMA to provide optimal data throughput for high speed applications. All ARINC 664 protocol operations, including VL traffic shaping, redundancy management, and IP fragmentation and reassembly, are handled onboard and require no host loading.



SOFTWARE SUPPORT

The PXIe-C664-V2 module is supported by AIT's ARINC 664 Software Development KIT (SDK) for Windows (XP, 7, 8, 10), Linux (Ubuntu & CentOS), and LabVIEW Real Time. It provides a robust Application Programmer's Interface (API) for read/ write access to the messaging ports and status information of the hardware module. Configuration of the simulated ARINC 664 End Systems (including the input/output VLs, upper protocol layers, and Sampling & Queuing message ports) is made easy with AIT's simple and intuitive Flight Simulyzer™ GUI application and XML based configuration data files. The PXIe-C664-V2 is also compatible with AIT ARINC 615A Software Data Loader tools allowing the module to be used for data loading target LRUs.

INPUT OPERATIONS

The PXIe-664-V2 module provides full on-board support for ARINC 664 integrity checking and redundancy management operations. These operations can be individually configured for each input VL, providing a flexible approach that supports a wide variety of data acquisition and analysis applications. In addition to supporting up to 512 input VLs the module can also be configured to operate in promiscuous mode to capture and record all network traffic. All captured data is time tagged.

The IP, UDP, and ARINC 653 upper protocol layers are fully

Key Features

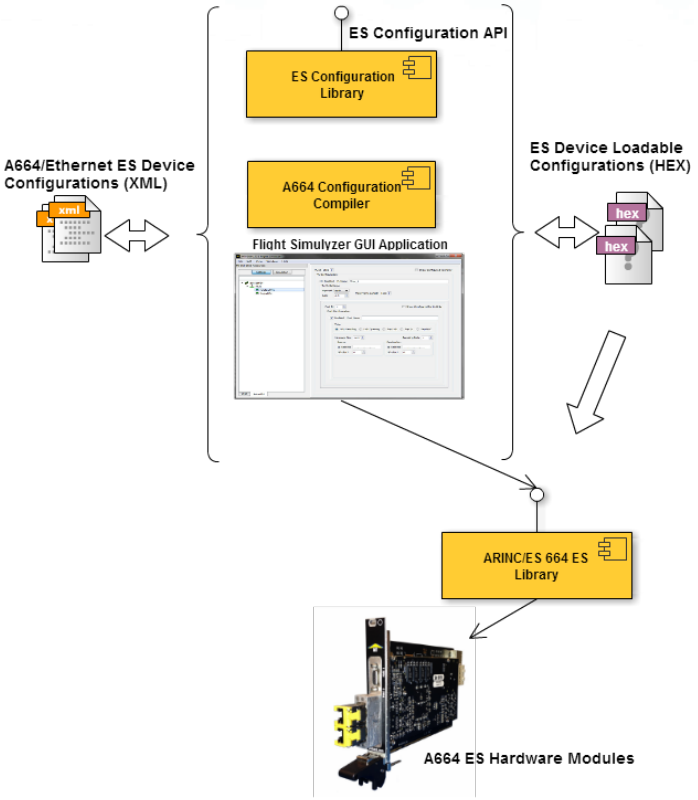
- IRIG 106 Chapter 10 output stream compatible with 3rd party recorders and telemetry tools
- Supports IEEE 802.3 10/100/1000 Mbit/s Full-Duplex Ethernet links
- Utilizes SFP's to support both copper and optical interfaces
- Simulates multiple ARINC 664 End Systems, including VL traffic shaping and input VL redundancy management
- Supports up to 128 Output VLs and 512 Input VLs with Sampling & Queuing Ports
- High Speed Ethernet data recording and replay
- Standard Ethernet operations simultaneous to ARINC 664 operations
- Upper layer protocol handling (ARINC 653, UDP, IP) managed onboard
- Time-stamping of all received messages with 8 nS resolution
- IRIG-B interface for coorelated timestamps accross modules and systems
- Windows XP/7/8/10, Linux, and LabVIEW Real Time Drivers & APIs provided (other OS support on request)
- Easy setup and configuration using AIT's Flight Simulyzer™ GUI application and XML based ARINC 664 End System configuration tools

managed onboard the PXIe-C664-V2. IP reassembly is fully managed by the module and requires no host loading or memory resources. The module supports up to 4096 input message ports. Each message port can be configured as ARINC 653 Sampling & Queuing ports, UDP Service Access Ports (SAP), IP Ports, or MAC ports providing the test application a flexible approach, allowing error detection and access to all protocol layers. The incoming messages to each port are buffered onboard and require no host resources.

OUTPUT OPERATIONS

The PXIe-664-V2 module allows the simulation of multiple ARINC 664 End Systems. The module can be configured to handle ARINC 664 VL traffic shapping for up to 128 output VLs. For each VL the source (MAC) address is individually configurable allowing output traffic to emulate multiple source End Systems.

The IP, UDP, and ARINC 653 upper protocol layers are fully managed onboard the PXIe-C664-V2. IP fragmentation is managed by the module, as well as VL sequence numbers and redundant data transmission, with no additional host loading. Up to 1024 output message ports are supported. The message ports can be configured as ARINC 653 Sampling & Queuing ports, UDP Service Access Ports (SAP), IP Ports, or MAC ports providing access to all protocol layers in support error injection and flexible output operations. Optionally, the module may be used in a replay mode to re-transmit previously captured network traffic.



ORDERING INFORMATION

PXIe-664-V2

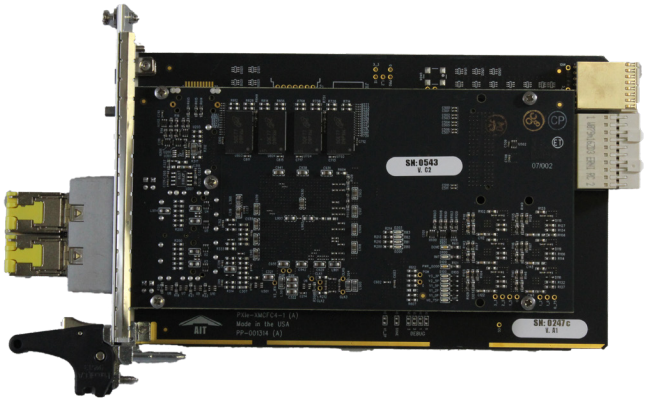
PXI Express module for ARINC 664 with two standard RJ-45 Ethernet network interfaces. Inlcudes IRIG-B Time Synchronization interface.

PXIe-664-V2-O

PXI Express module for ARINC 664 with two optical Ethernet network interfaces. Inlcudes IRIG-B Time Synchronization interface.

F-SIM-A664

Flight Simulyzer™ ARINC 664 ES Configuration application and analyzer



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